Les Banki Circuit
Updated Version
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Synchronized 3 Frequency PWM circuit & cell drivers

(for 'resonance' electrolysis of water)

Background

The basic idea for this design is based on information published by Bob Boyce.
(He is a member of several 'free energy' discussion groups/forums on Internet.)
Amongst many other very useful bits of information, he has revealed the frequencies, the 'feed' method to the
electrolyzer cell & other important electronic details.

Having been heavily involved in the "water fuel" technology (about 13 years ago) I can easily tell if published
information bits are dis-information or REAL.
I have collected some of Bob's most important postings and put them in a file (about 78 pages, at present) I
simply named 'Bob Boyce'.
I am convinced that he is possibly the most knowledgeable man (alive), with practical knowledge, on the
subject of using water as the ONLY fuel.

This also happens to be my goal. (NO mixing with any other type of fuel to buy!)

Introduction

In more than one posting, Bob has stated that there should (ideally) be 3 frequencies, harmonically related, to
obtain optimum results.
These centre frequencies are: 10.7kHz – 21.4kHz – 42.8kHz
They should NOT be in phase but very, very close (slight phase delay between them).
These frequencies could/should be mixed ('modulated') in a transformer which feeds the electrolyzer cell from
its secondary winding.
(However, he added that tuning 3 independent frequencies simultaneously is not an easy task. The details above
may explain why so many experimenters in the past have failed to obtain results in their quest of finding the
"resonance" frequency of water.)

Brief technical description

My basic idea is as follows: Since the frequencies: 10.7kHz – 21.4kHz – 42.8kHz are harmonically related, only
ONE needs to be tuned.
Either frequency multiplication or division can be performed to obtain the other two. (Using flip-flops, digital
division is very simple.)

Using division, we start with the highest frequency, 42.8kHz.
Divide by two gives 21.4kHz. Divide that by two gives 10.7kHz.
There are two remaining tasks to be performed:
Synchronizing the 3 independent PWM oscillators running at F, F/2, F/4) and,
provide adjustable phase delays between them.

My design is based on the SG3525A, (a regulating PWM chip) because of its following features:
* Oscillator frequency range: 100Hz – 400kHz
* It has an 'oscillator output' terminal

* Separate 'sync' terminal [multiple units can be 'slaved' (synchronized)]
* Internal 'soft start'
* Pulse-by-pulse 'shut down'
* Adjustable dead-time control
* Latching PWM to prevent multiple pulses
* Totem-pole, dual source/sink output drivers
* Input under voltage lockout with hysteresis
* Its outputs can be configured as single-ended OR push-pull

The SG3525A is also cheap and readily available.

Further, it should be obvious to the technical reader, that any other group of frequencies can be used by the
appropriate choice of time constants for the oscillators, phase delays and sync pulses – within the limits of the
SG3525's oscillator frequency range.

A single 4013 (CMOS, dual D-type flip-flop IC) performs the 2 frequency divisions.
Two 4538 (CMOS, dual monostable multivibrator, in non-retriggerable modes),
act as phase delays and sync pulse generators at the same time.

With this arrangement, adjustments have been greatly simplified:

* Only ONE (the highest) frequency is 'tuned'.
(The other two are automatically 'locked' to be F/2 and F/4.)
* Duty Cycle for all 3 Pulse Width Modulators can be set independently or, with a common control to the same
value – as desired.
* The two phase delays can be independently adjusted between pre-determined limits.
* All 3 PWM outputs can be configured as single-ended OR push-pull drive, as desired.
(Note: transformer windings needs to match - single-ended OR push-pull- respectively.)

Detailed technical description:

I will not describe/explain the internal circuitry of the SG3525 PWM as it is well covered by Application Note
AN250/1188 by SGS-THOMSON MICROELECTRONICS.

AN230/1188 by SGS-THOMSON MICROELECTRONICS.
I will only deal with the chip's important features and how they are used in this design.

The main feature for this application is the ability to 'synchronize' multiple chips.
The 'twist' here is that the two 'slave' units are tuned/synchronized to generate
F/2 and F/4 sub-harmonics.
This is the way its done:
IC1's 'oscillator output' (pin 4) signal is amplified by a single transistor TR4 (BC547) since its amplitude is too
low for driving the CMOS IC's input.
(this single transistor stage inverts the pulses but that does not matter here)
This amplified oscillator output signal is fed to the clock input (pin 3) of IC4A (4013).
The F/2 output (now a 'square wave' with ~ 50% duty cycle) from pin 1 (Q output) is fed to the clock input (pin
11) of the second flip-flop (IC4B) and also to the "A"
(rising edge input, pin 4) of IC5A (4538)

IC5A generates the 'phase delay' pulses.
The R-C time constant is determined by C22 (1n), R18 (12k) and P5 (10k)
[Note: the specified minimum output pulse width for the 4538 is 1   s. Therefore, a small (say 1 or 2 phase
shift at the frequencies involved here) can not be generated directly.]
So, the phase is delayed by around 180 which can then be fine tuned to the required amount. Note also that

with this method not only phase 'lag' but also phase 'lead' can be easily set within very wide limits!
Needless to say that since the phase shift is naturally frequency dependent, altering the frequency will (slightly)
alter the phase shift.

The 'Q' output of IC5A (pin 6) is connected to the second non-retriggerable monostable's (IC5B) "B" input (pin
11, falling edge trigger).

IC5B is the sync pulse generator.
The R-C time constant C23 (100p) and R19 (3.9k) set the pulse width to about 390ns.
From the 'Q' output (pin 10) these pulses are fed to the 'sync' input (pin3) of IC2 (second PWM IC, SG3525A)
Its oscillator time constant [C17 (10n), R7 (8.2k) & R9 (33ohm)] is set to be about 10% longer than the
minimum expected frequency.
It should be noted here that the oscillator timing capacitors C17 & C21 do not begin to recharge as long as their
sync pins are high.
In other words, these oscillators do not start before the sync pulses are terminated.

The second 'divider/phase delay/sync pulse generator' stage for the 3rd PWM (IC3) is identical to the first one,
with the addition of IC6 (A & B)
The only difference is that the F/2 pulses are taken from the 'Q' output (pin 1) of IC4A and fed to the clock
input (pin 11) of the second divider flip-flop, IC4B.

P1 is the ONLY frequency control. With the component values shown in the diagram, it has a range of approx.
+7.5% to -6.5% from the centre frequency of 42.8kHz. The other two PWM oscillators are in sync, giving
EXACTLY F/2 and F/4.

Pulse Width Modulation (Duty Cycle) is either adjusted individually with P2, P3 and P4, or collectively, by P2
(50k), connecting the slider (through 10k resistors) to pin 2 of IC1, IC2 and IC3. (In that case, P3 and P4 are
omitted.)
The SG3525A's control voltage (for duty cycle adjustment) ranges from about 0.9V to 3.3V (typical).
Setting this control voltage range minimizes the 'dead band' of the potentiometer.

The 1V – 3.3V range is set by the bias network [D4, D5, D6, D7, R1 (39k) - P1 (50k) - P2 (50k) – P3 (50k) –
D8, D9] between the 5.1V reference voltage (pin 16 of IC1) and ground.
The outputs of the 3 Pulse Width Modulators [IC1, IC2 & IC3 (SG3525)] are arranged as single ended outputs
by connecting their A & B outputs (pins 11 & 14) to ground and using the 'Vc' (pin 13) as output with pull-up
resistors R4, R8 & R12 (1k) to the positive supply rail.

Using a dedicated MOSFET driver have some advantages compared to the use of complementary discrete
transistors.
First of all, the TC 4420 MOSFET driver can supply peak currents of up to 6A! to the gate of the MOSFET
switch.
Second, when using this driver, there is no need for level shifting.
Since it has a 'Schmitt trigger' input, it also acts as a 'wave shaper'.
But perhaps most importantly, there is no need to amplify the pulses.
(That would involve yet another IC, a wide band OP. To fully turn on most power MOSFETS, a drive voltage of
at least 10 – 12V is needed.)

TVS diodes D1, D2 and D3 (1.5KE18A) are protecting the MOSFETS.
They are SUPER FAST devices, working in the sub-nanosecond (pico) range!

[Users of the TC4420/TC4429 Universal Power MOSFET Interface Ic's should be aware that for trouble free
performance, a careful printed circuit board layout is essential, especially de-coupling and grounding.